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10EC56

Fifth Semester B.E. Degree Examination, Dec.2017/Jan.2018
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions, selecting at least TWO questions from each part.***
2. ***Draw Neat diagram.***

PART – A

1 a. Describe with neat diagrams, the P-well fabrication process. **(08 Marks)**

b. Explain the DC transfer characteristics of CMOS inverter and mark all the regions of operation with necessary expressions for V_{out} in each region. **(08 Marks)**

c. Compare CMOS and Bipolar Technology. **(04 Marks)**

2 a. Explain Transmission gate and Tristate inverter operations with neat diagram. **(06 Marks)**

b. Give the λ-based design rules for different layers, p and n MOSFETS and contact cuts. **(08 Marks)**

c. Obtain the stick diagram and layout of two way selector with enable. **(06 Marks)**

3 a. What are the features of CMOS Domino logic? Explain with neat diagram. **(06 Marks)**

b. In the following circuit find V_1, V_2, V_3 and V_4. **(06 Marks)**

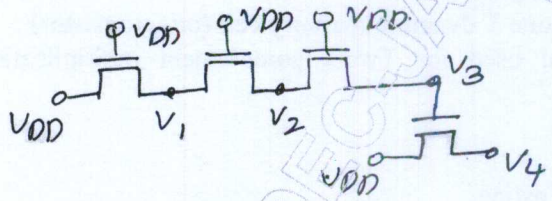

Fig Q3(b) 1

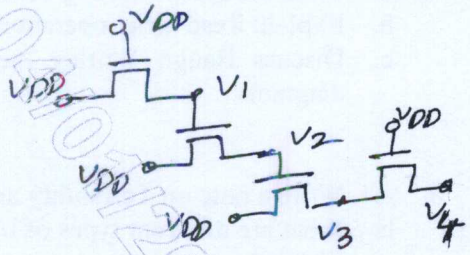

Fig Q3(b) 2

c. Explain following logic structure with their salient features with neat diagram
i) Pseudo nMOS logic
ii) C^2MOS logic **(08 Marks)**

4 a. Define sheet Resistance and standard unit of capacitance □Cg. **(06 Marks)**

b. Explain cascaded inverter to drive large capacitance loads? Obtain an equation to find the number of stages. **(08 Marks)**

c. Calculate the total capacitance in terms of □Cg for the following Fig.Q4(c) **(06 Marks)**

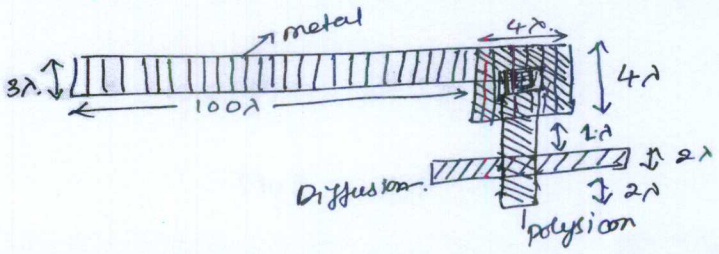

Fig Q4(c)

PART – B

5 a. What are the properties of nMOS and PMOS switches? How TG is useful. **(06 Marks)**

b. Explain the structure design of a parity generation with necessary diagrams and also write stick diagrams. **(08 Marks)**

c. Obtain the logic implementation of 4-way multiplexer (Selector) using nMOS switches with necessary diagrams. **(06 Marks)**

6 a. Explain nMOS and CMOS non-inverting dynamic storage cell and draw the 4-bit shift register using nMOS. **(07 Marks)**

b. How to implement arithmetic and logic operation with a standard adder? Explain with the help of logic expression. **(06 Marks)**

c. Explain 4×4 Barrel shifter with neat diagram. **(07 Marks)**

7 a. What are system timing consideration? **(05 Marks)**

b. Explain Read/write operation of one T dynamic memory cell (one transistor). **(05 Marks)**

c. Discuss Baugh Worley method used for Two's complement multiplication with neat diagrams. **(10 Marks)**

8 a. Write a note on Testability and Testing. **(06 Marks)**

b. What are different types of I/O pads? **(06 Marks)**

c. Write short notes on :

i) Built in self Test (BIST)

ii) Scan design Technic. **(08 Marks)**

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